REMARKS

Reconsideration of the application is respectfully requested.

Claim Rejections – 35 U.S.C. §102

Claims 1-3, 6-9, and 17-24 stand rejected as being anticipated by U.S. Patent No. 6,407,960 issued to Egbert, et al. ("Egbert").

With respect to claim 1, Applicants have amended this claim to overcome the rejection. Although Egbert shows an arrangement for programming selected device registers 12 of an integrated device 10, from an external memory 14, Egbert does not teach or suggest a method in which an indication is received that an attempt has been made to access a first register within an integrated circuit (IC) component, where the first register reflects an index variable that points to a configuration register of the IC component.

For instance, assuming Applicants' claimed *first register* reads on the EEPROM 14 location 000 and Applicants' claimed *second register* reads on the location 0001, Egbert does not teach or suggest the operations of receiving the indications as recited in claim 1, including without waiting for another attempt to access the first register, changing the index variable to point to another configuration register of the IC component. Accordingly, reconsideration and withdrawal of the rejection of claim 1 is requested.

As to claim 7, this claim stands rejected based on the assertion that, in the context of claim 7, Applicants' claimed *second control register* reads on reference 28 at address 0001 of EEPROM 14. However, that is an improper rejection because the arrangement in Egbert does not **write** to this location a *further content value for another selected one of the configuration registers*. The integrated device 10 only **reads** from the location in EEPROM 14. Also, the Office Action subsequently, at page 4, takes the position that **another** location, namely AV2 (reference 26) is Applicant's *second register*. The Office Action cannot have it both ways, where on the one hand Egbert is said to teach Applicants' claimed *second control register* as D1, which is the content for register A1, and simultaneously AV2. D1 is the content of the first register A1, while D2 and AV2 are associated with a different second register A2. Accordingly, because Egbert does

not teach or suggest *writing to the second control register a further content value for another selected one of the registers, without again writing to the first control register,* Egbert does not anticipate claim 7.

Claim Rejections - 35 U.S.C. §103

The next independent claim, claim 10, stands rejected as being obvious over Egbert and the level of ordinary skill in the art. It is contended in the Office Action that Egbert teaches claim 10's *detection logic having an input to receive a first hardware control signal that indicates a request has been received from outside of the IC component to access a configuration register and an output to provide an increment or decrement signal to the counter.* The Office Action points to Fig. 1 of Egbert, element 18 which is described in Egbert as a memory sensor that determines the presence of the connected external memory 14.

However, the memory sensor 18 does not have *an input to receive a first hardware control signal that indicates a request has been received from outside of the IC component to access a configuration register.* The sensor 18 is part of an external memory interface 16 that is configured **for reading the values of the external memory 14 via a serial data output connection (EEDO). The external memory interface 16 also includes pin connections for a chip select signal (EECS), a serial clock (EESK), and a serial data input (EEDI) used for programming of the external memory**. None of these control signals is used to indicate that a request has been received from outside of the integrated device 10 to access a configuration register. Rather, it is the integrated device 10 that must initiate a read from the external memory, to program its own configuration registers. Thus, any request to access the configuration register in the integrated device 10 comes from within the device 10, not the EEPROM 14. [Egbert, col. 3, lines 7-13] Accordingly, since Egbert does not teach or suggest the claimed *detection logic,* and no other reference has been relied upon as teaching such a limitation, reconsideration and withdrawal of the obviousness rejection of claim 10 is requested.

As to claim 13, this claim also recites *detection logic having an input to receive a first hardware control signal that indicates a request has been received from outside of the I/O hub to access a configuration register, and an output to provide an increment or decrement counter signal,* and since such a limitation is not taught by either Egbert or other references

relied upon in the Office Action, reconsideration and withdrawal of the rejection of claim 13 is requested.

Claim 17 recites a method for programming software-accessible registers in which a first bus event is detected, which is aimed at accessing an index variable that points to one of a number of registers of the system, and a second bus event that is aimed at accessing the content of the register to which the index variable points. Thus, two separate bus events are detected. One is aimed at accessing an index variable and the other is aimed at accessing the content of the register pointed to by the index variable. This particular detection of bus events is not taught or suggested in Egbert.

In Egbert, an external memory is read by a controller device 10, in response to detecting the presence of the external memory during power on reset (Fig. 2, block 50). A register address value is read from a particular external memory location (block 52). The next step involving an access between the controller and the external memory is block 58, in which a register data value is read (from the next external memory location). Even if we assume block 52 teaches the *detection of a bus event* as in Applicants' claim 17, no other bus events are detected. There is no teaching or suggestion that *a second bus event aimed at accessing the content of the register to which the index variable points is detected.* Merely reading a register data value from the next memory location (block 58) does not teach or suggest Applicants' claimed detection operations. Accordingly, since Egbert does not teach or suggest at least the detection operations of claim 17, claim 17 is not anticipated by Egbert.

The final independent claim, claim 22, is directed to giving a machine the capability to initiate a block mode of operation in which a number of configuration registers are programmed in accordance with certain bus transactions. A bus transaction is to access a first control register, and another bus transaction is to access a second control register. Then, a number of further bus transactions each to access the second control register without any further bus transactions to access the first control register are to occur. This is not taught or suggested by Egbert.

In Egbert, even if we assume that a bus transaction occurs when the integrated device 10 reads from the EEPROM 14 the contents of a location (be it either an address

value AV or a data value D), **every one of the registers 12 in the integrated device 10 calls for both a transaction to read a new address value and a transaction to read a new data value**. This does not teach or suggest Applicants' process in which *a plurality of further bus transactions each to access the second control register without any further bus transactions to access the first control register* are to occur. This is also referred to as Applicants' *block mode of operation* in which a number of configuration registers are sequentially programmed without any bus transactions needed to update the first control register (but that bus transactions are needed to access the second control register). This block mode of operation is not taught or suggested by Egbert. Thus, claim 22 is not anticipated by Egbert. Nevertheless, Applicants have amended claim 22 to clarify a particular embodiment of the invention in which the first control register is to point to any one of the configuration registers, and the second control register reflects the content of any one of the configuration registers. Even if we assume that such registers could be added to the integrated device 10, Egbert and the relied upon art references do not teach or suggest the claimed block mode of operation involving such registers. Accordingly, claim 22 is not anticipated or obvious for those additional reasons.

Any dependent claims not mentioned above are submitted as not being anticipated or obvious, for at least the same reasons given above in support of their base claims.

It should be noted that not all of the assertions made in the Office Action, particularly those with respect to the dependent claims, have been addressed here, in the interest of conciseness. Applicants reserve the right to challenge any of the assertions made in the Office Action by the Examiner, with respect to the relied upon art references and how they would relate to Applicants' claim language.

CONCLUSION

In sum, a good faith attempt has been made to explain why the rejection of the claims is improper, and how the claims are believed to be in condition for allowance. A Notice of Allowance referring to claims 1-24, as amended here, is therefore respectfully requested to issue at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: June 30, 2006

By _____
Farzad E. Amini, Reg. No. 42,261

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on June 30, 2006.

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Margaux Rodriguez *June 30, 2006*